Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Ti/Ni/V/Ag**

**Bond Pad Size: S = .041” X .139” G = .007” X .007”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .093” X .145” DATE: 4/25/22**

**MFG: FAIRCHILD THICKNESS .008” P/N: FDS8638**

**DG 10.1.2**

#### Rev B, 7/19/02